

Claims

- [c1] 1. A high speed programmable divider circuit with symmetrical duty cycle, comprising:
- a division mode controller capable of specifying a binary encoded divisor value;
 - a linear feedback shift register (LFSR) coupled to the division mode controller and forming a first stage divide function;
 - a master-slave latch coupled in series with the LFSR and forming a second stage divide function;
 - a duty cycle correction circuit coupled in series with the master-slave latch; and
 - an inverter with an input coupled to a slave output of the master-slave latch and to the duty cycle correction circuit and an output coupled to the division mode controller and the data input of the master-slave latch.
- [c2] 2. The high speed programmable divider circuit according to claim 1, wherein the division mode controller is adapted to alternate the divisor value every clock cycle by one more or one less than a desired final divisor value for an odd numbered final divisor value.

[c3] 3. The high speed programmable divider circuit according to claim 1, further comprising:

- a logic gate coupled to the LFSR output and driving the second divider element; and
- a latch controlling a final divide value of the division mode controller.

[c4] 4. The high speed programmable divider circuit according to claim 1, wherein the LFSR comprises:

- a plurality of series coupled latch elements forming a counter capable of producing an odd number of counter states;
- a pipeline latch element coupled in parallel with one of the plurality of latch elements;
- a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and
- an output logic element coupled to the outputs of each of the plurality of latch elements of the counter, the output logic element capable of detecting a complete cycle of the counter states.

[c5] 5. The high speed programmable divider circuit accord-

ing to claim 3, wherein the second divide element comprises a divide-by-two latch.

[c6] 6. The high speed programmable divider circuit according to claim 3, wherein the second divide element comprises a divide-by-four latch pair.

[c7] 7. The high speed programmable divider circuit according to claim 3, wherein the second divide element comprises a plurality of m latches, where m is an even integer.

[c8] 8. The high speed programmable divider circuit according to claim 7, wherein the second divider stage includes a plurality of multiplexor elements to control phase alignment of the output of the frequency divider.

[c9] 9. The high speed programmable divider circuit according to claim 8, further comprising:
a second divider circuit coupled in parallel with the programmable frequency divider and forming a multiple divider; and
a synchronization circuit coupled to the multiple divider capable of detecting synchronization of output transitions from the multiple divider and generating a synchronization signal.

[c10] 10. The high speed programmable divider circuit of

claim 9, wherein the second divider specifies a final divisor that is different from the frequency divider.

[c11] 11. A method of performing a frequency division of a digital waveform, the method comprising:

- specifying a binary encoded divisor using a division mode controller;
- forming a first stage divide function using a linear feedback shift register coupled to the division mode controller and;
- forming a second stage divide function using a master-slave latch coupled in series with the LFSR and;
- generating a symmetrical output of the frequency division output using a duty cycle correction circuit coupled in series with the master/slave latch;
- selecting a divisor value of the LFSR as a function of a desired final divisor value to perform an even or an odd divide-by function;
- alternating the divisor value of the LFSR by one more or one less than the desired final divisor value for an odd numbered final divisor value; and
- maintaining the divisor value of the LFSR for an even numbered final divisor value.

[c12] 12. The method according to claim 11 further comprising:

- changing the final divisor value synchronously with

an output pulse of the LFSR.

[c13] 13. The method according to claim 11, further comprising:

forming a multiple divider circuit by operating a second frequency divider in parallel with the frequency divider;

synchronizing the outputs of the multiple divider;
and

maintaining a specified phase relationship between the frequency divider and the second frequency divider.

[c14] 14. A high speed linear feedback shift register (LFSR), comprising:

a plurality of series coupled latch elements forming a counter capable of producing an odd number of counter states;

a pipeline latch element coupled in parallel with one of the plurality of latch elements;

a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and

an output logic element coupled to the outputs of

each of the plurality of latch elements of the counter, the output logic element capable of detecting a complete cycle of the counter states.

- [c15] 15. A high speed linear feedback shift register (LFSR), comprising:
- a first plurality of series coupled latch elements forming a first counter capable of producing an odd number of counter states;
 - a second plurality of series coupled latch elements coupled in parallel with the first plurality of latch elements, the second plurality of latch elements forming a second counter capable of producing an even number of counter states;
 - a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the first counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and
 - an output logic element coupled to the outputs of each of the plurality of latch elements of the first counter and the second counter, the output logic element capable of detecting a complete cycle of the LFSR counter states.

- [c16] 16. The high speed LFSR according to claim 15, wherein the second counter element comprises a divide-by-two latch.
- [c17] 17. The high speed LFSR according to claim 15, wherein the second counter element comprises a divide-by-four latch pair.
- [c18] 18. The high speed LFSR according to claim 15, wherein the second counter element comprises a divide-by- n latch, where n is an even integer.
- [c19] 19. The high speed programmable divider circuit according to claim 15, wherein the feedback logic network comprises an XOR gate coupled to an output of a first LFSR latch and to the output of a second LFSR latch and to the input of a third LFSR latch.
- [c20] 20. The high speed LFSR according to claim 19, wherein the logic function of the XOR gate is decomposed into multiple logic stages and distributed across multiple latch elements of the first counter such that a maximum latch-to-latch operational latency of the LFSR does not exceed one gate delay.
- [c21] 21. The high speed LFSR according to claim 14, wherein the feedback logic network comprises:
a network of XOR gates distributed across multiple

latch elements of the first counter such that a maximum latch-to-latch operational latency does not exceed one XOR gate delay; and
a first pipeline latch element accepting an output from a first XOR gate, the pipeline latch element being coupled in parallel with one of the first plurality of latch elements.

[c22] 22. A high speed linear feedback shift register, comprising:

a plurality of series coupled latch elements forming a first counter capable of producing an odd number of counter states;

a second counter coupled in parallel with the first counter, the second counter capable of producing an even number of counter states;

a multi-stage feedback logic network distributed across the plurality of latch elements of the first counter such that the maximum latch-to-latch operational latency of the first counter does not exceed one gate delay;

a first pipeline latch capable of storing a first parallel output of a first stage of the feedback logic network, the first pipeline latch coupled in parallel with one of the plurality of latch elements of the first counter;
and

an output logic element coupled to the outputs of each of the plurality of latch elements of the first counter, the output logic element adapted to detect a unique counter state of the LFSR.

[c23] 23. The high speed LFSR according to claim 22, wherein the multistage feedback network includes a second logic stage coupled between a first latch element and a second latch element of the plurality of latch elements of the first counter.

[c24] 24. The high speed LFSR according to claim 22, further comprising:
a plurality of multiplexor elements corresponding to each of the plurality of latch elements of the first counter, the multiplexor elements providing a programming function of the LFSR;
a latch element controlling the multiplexor elements;
and
a reset latch coupled to the output logic element.

[c25] 25. A method of forming a high speed LFSR, the method comprising:
forming a first counter capable of producing an odd number of counter states using a first plurality of series coupled latch elements;
forming a second counter capable of producing an

even number of counter states using a second plurality of series coupled latch elements coupled in parallel with the first plurality of latch elements; generating a primitive polynomial using a feedback logic network decomposed into multiple logic stages; distributing a feedback logic network across multiple latch elements of the first counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay; storing a first parallel output of a first stage of the feedback logic network in a first pipeline latch coupled in parallel with one of the plurality of latch elements of the first counter; and detecting a complete cycle of the LFSR counter states using an output logic element coupled to the outputs of each of the plurality of latch elements of the first counter and the second counter.